

ASSP

1 CHANNEL 10-BIT D/A CONVERTER

MB40730

MB40730 is a low-power consumption, high-speed 10-bit D/A converter.

The MB40730 is characterized by ECL (10 kH) compatible digital inputs, an analog output voltage from -2 to 0 V, and a maximum conversion rate of 60 MHz. It provides a reference voltage from a potential divider and band-gap reference, and can also use an external reference voltage.

The MB40730 D/A converter is suitable for high-resolution TVs or VTRs.

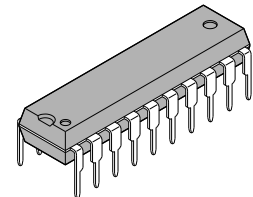
- Resolution: 10 bits
- Conversion characteristics:
 - Maximum conversion rate: 60 MHz (Minimum)
 - Linearity error: $\pm 0.1\%$ (Maximum)
 - Differential linearity error: $\pm 0.1\%$ (Maximum)
- Input and output:
 - Digital input voltage: ECL (10 kH) levels
 - Analog output voltage: 2 Vp-p (-2 V to 0 V)
- Reference voltage:
 - V_{ROUT1}: Potential divider circuit ($V_{EEA} \times 2/5.2$)
 - V_{ROUT2}: Band-gap reference circuit (-2 V)
- Others:
 - Supply voltage: -5.2 V single power supply
 - Power dissipation: 180 mW (Typical value at analog output voltage 2 Vp-p)
 - 140 mW (Typical value at analog output voltage 1 Vp-p)

ABSOLUTE MAXIMUM RATINGS (See NOTE)

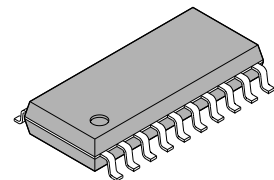
(V_{CCA}=V_{CCD}=0 V, T_a=+25°C)

Parameter	Symbol	Value	Unit
Analog power supply voltage	V _{EEA}	-7.0 to 0	V
Digital power supply voltage	V _{EED}	-7.0 to 0	V
Power supply voltage difference	V _{EED} -V _{EEA}	1.0	V
Digital signal input voltage	V _{ID}	0 to V _{EE}	V
Storage Temperature	T _{stg}	-55 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Rating** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

20-PIN PLASTIC DIP

(DIP-20P-M01)

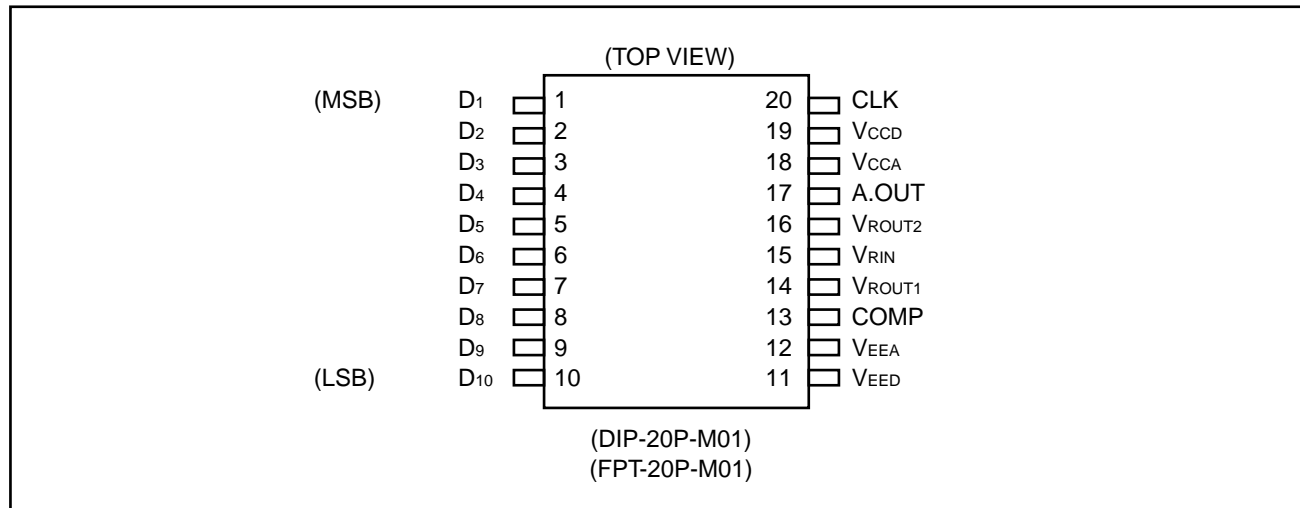
20-PIN PLASTIC SOP

(FPT-20P-M01)

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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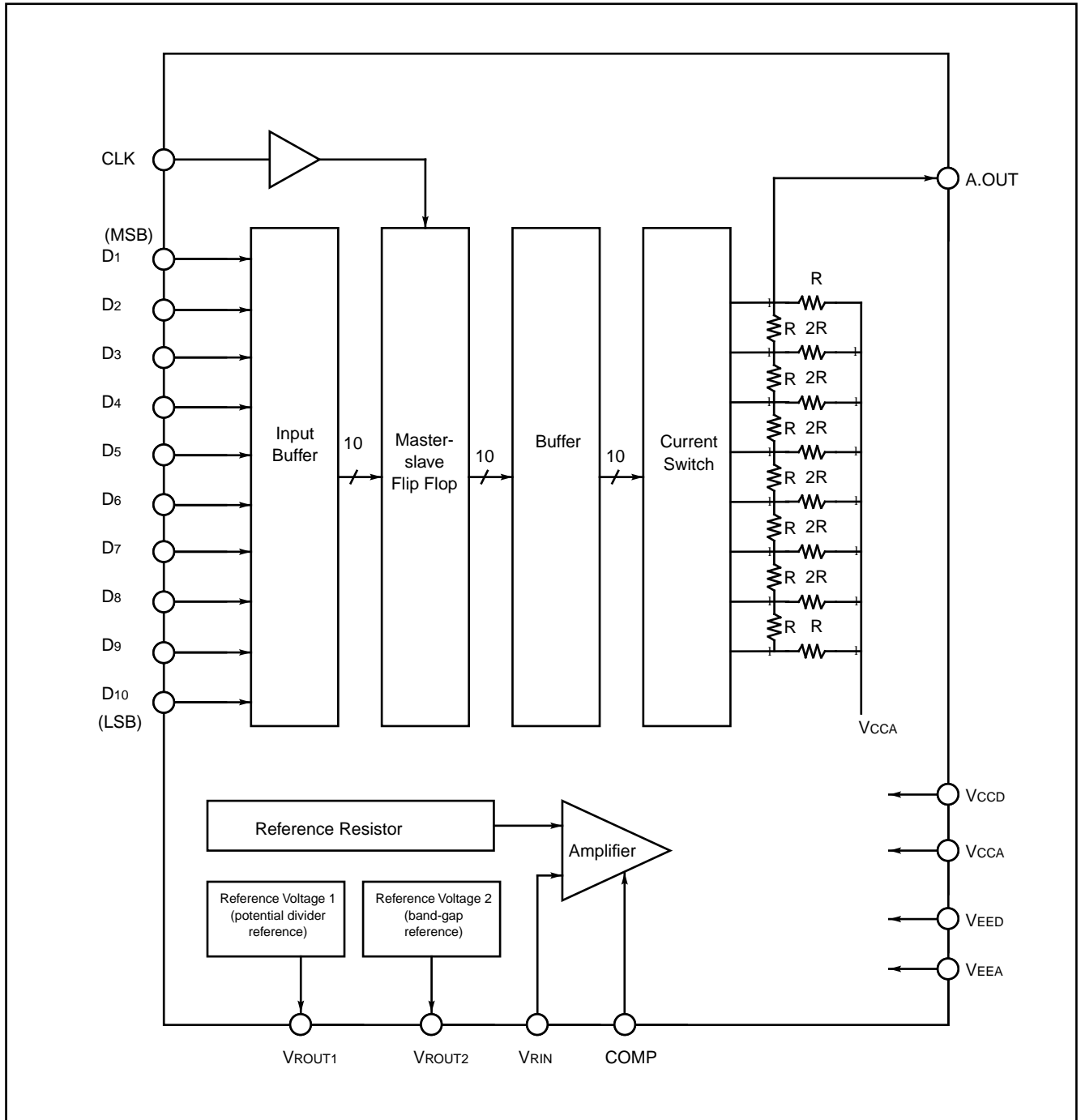
■ PIN ASSIGNMENT



■ PIN DESCRIPTIONS

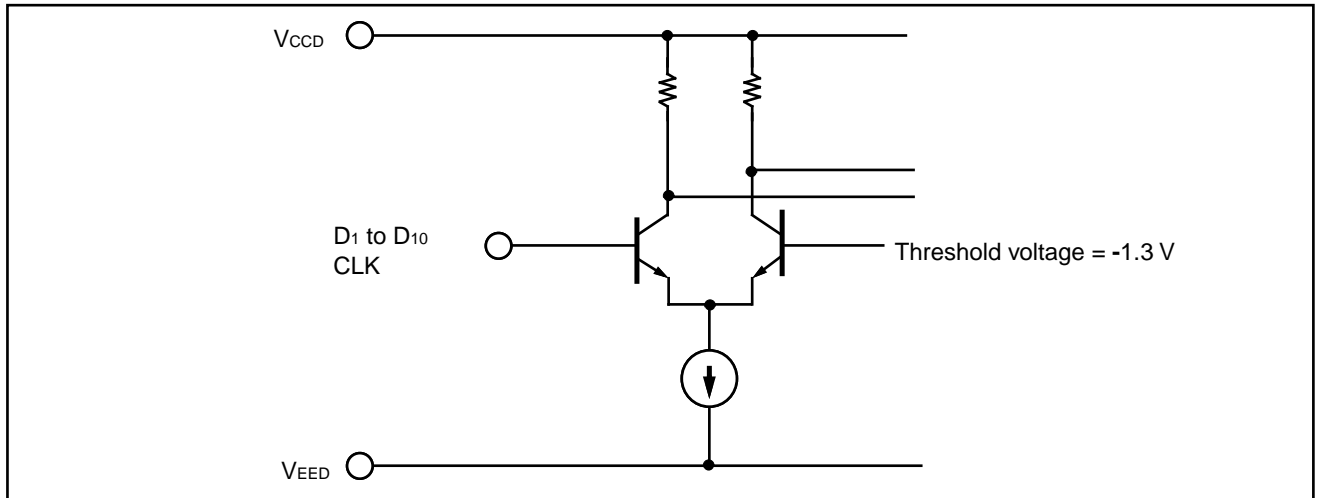
Pin No.	Symbol	I/O	Description
1 to 10	D ₁ to D ₁₀	I	Data signal input pin (D ₁ : MSB, D ₁₀ : LSB)
20	CLK	I	Clock signal input pin
19	VCCD	-	Digital ground pin (0 V)
18	VCCA	-	Analog ground pin (0 V)
11	VEED	-	Digital power pin (-5.2 V)
12	VEEA	-	Analog ground pin (-5.2 V)
15	VRIN	I	Reference voltage input pin Analog output dynamic range setup pin Connect to pin 14 or 16 to use the built-in reference voltage When using an external reference voltage, the voltage on this pin must be from -2.20 V to -0.70 V
14	VROUT1	O	Reference voltage output pin 1 The output voltage of the potential divider reference is fixed at $V_{EEA} \cdot 2/5.2$. When this pin is connected to pin 15, the analog output voltage ranges from $V_{EEA} \cdot 2/5.2$ to 0 V
16	VROUT2	O	Reference voltage output pin 2 The output voltage of the band-gap reference is fixed at -2.0 V. When the pin is connected to pin 15, the analog output voltage ranges from -2 V to 0 V
13	COMP	-	Phase compensation capacitor pin Insert a capacitor of 0.1 μ F or greater between VEEA and COMP for phase compensation
17	A. OUT	O	Analog signal output pin

■ BLOCK DIAGRAM

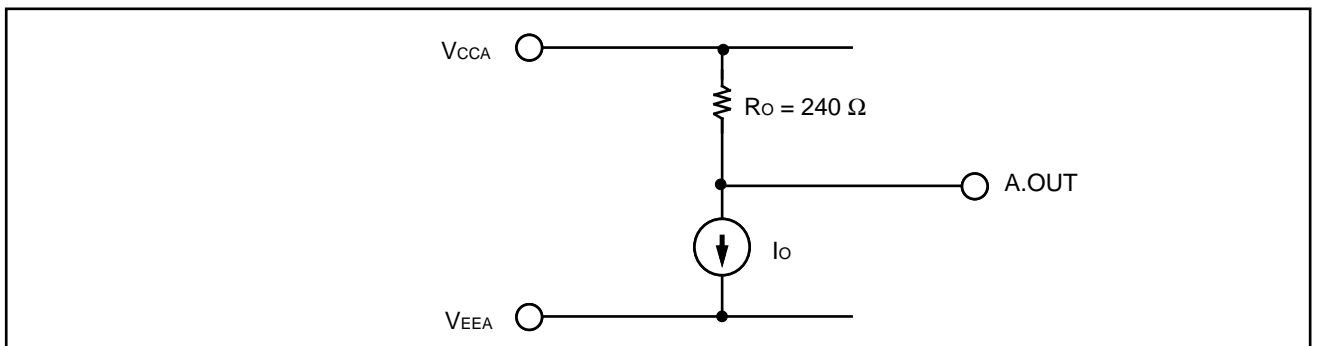


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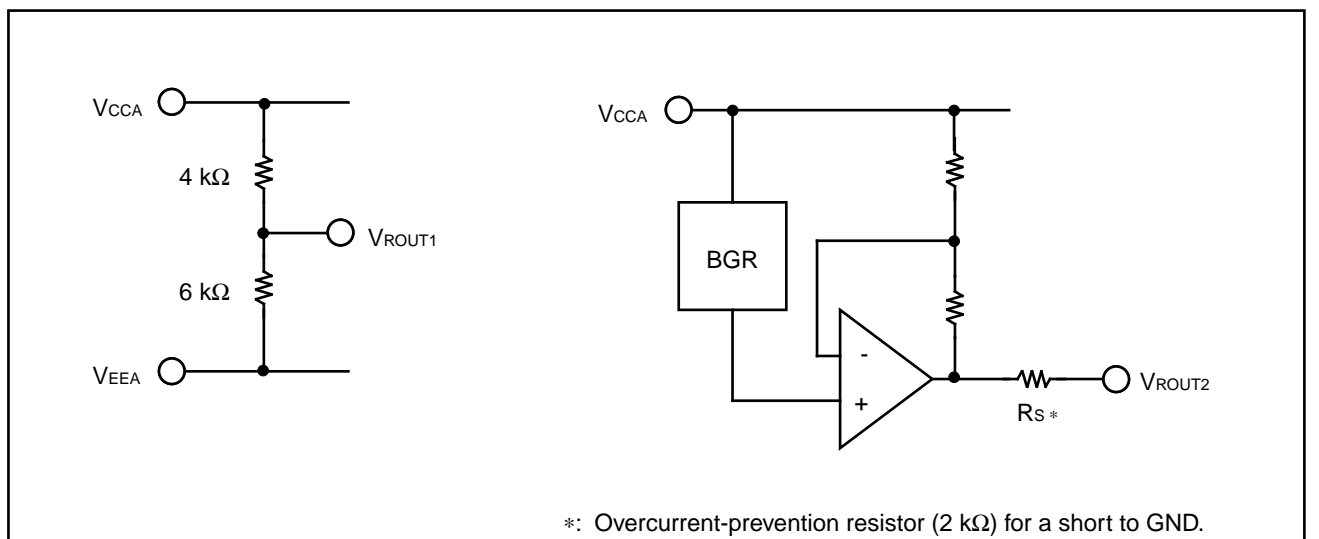
■ DIGITAL INPUT EQUIVALENT CIRCUIT



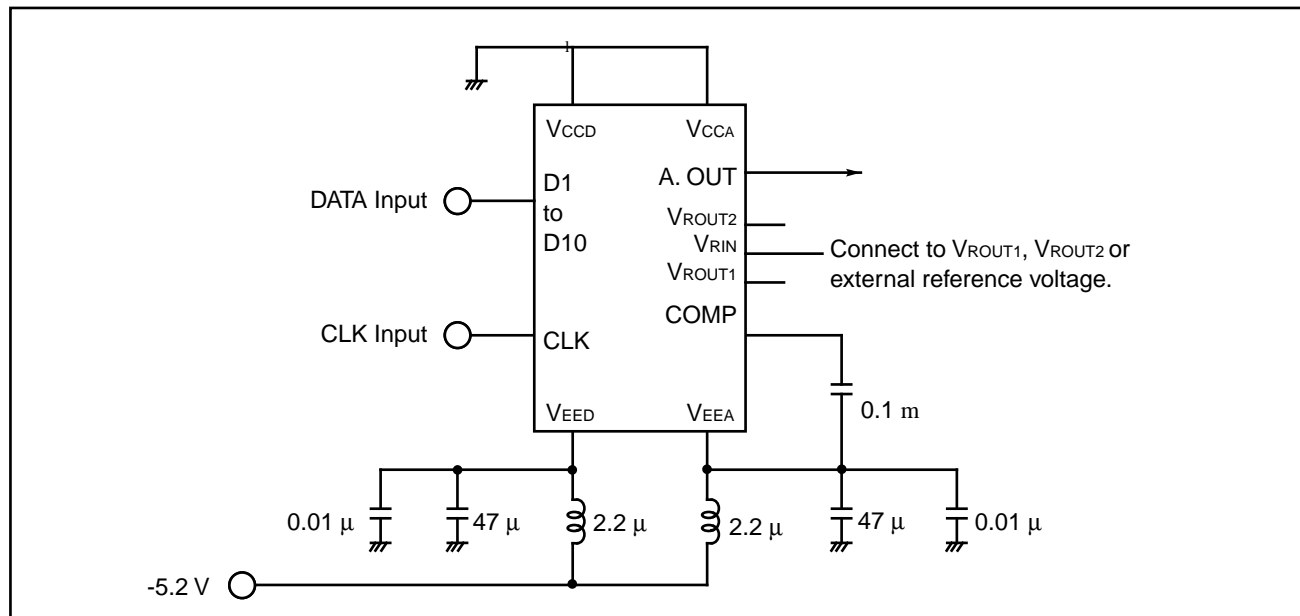
■ ANALOG OUTPUT EQUIVALENT CIRCUIT



■ REFERENCE VOLTAGE OUTPUT EQUIVALENT CIRCUIT



■ TYPICAL CONNECTION EXAMPLE



■ RECOMMENDED OPERATING CONDITIONS

(VCCA=VCCD=0 V, Ta=-20°C to +75°C)

Parameter		Symbol	Standard value			Unit
			Min.	Typ.	Max.	
Power supply voltage	Analog power supply voltage	VEEA	-5.46	-5.20	-4.94	V
	Digital power supply voltage	VEED	-5.46	-5.20	-4.94	V
	Power supply voltage difference	VEEA-VEED	-0.2	-	0.2	V
Analog reference voltage		VRIN	-2.20	-2.00	-0.70	V
Digital input high voltage	VIHD	-20°C	-	-	-0.88	V
		25°C	-1.13	-	-0.81	V
		75°C	-	-	-0.735	V
Digital input low voltage	VILD	-20°C	-1.95	-	-	V
		25°C	-1.95	-	-1.48	V
		75°C	-1.95	-	-	V
Clock frequency		fCLK	-	-	60	MHz
Setup time		tsu	8	-	-	ns
Hold time		th	2	-	-	ns
Clock minimum pulse width high		twH	6.5	-	-	ns
Clock minimum pulse width low		twL	6.5	-	-	ns
Phase compensation capacitor		C _{COMP}	0.1	-	-	μF
Operating temperature		T _{op}	-20	-	75	°C

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■ DC CHARACTERISTICS

(V_{EEA}=V_{VEED}=-5.46 to -4.94 V, T_a=-20°C to +75°C)

Parameter	Symbol	Condition	Standard values			Unit	
			Min.	Typ.	Max.		
Resolution	-	-	-	-	10	bit	
Linearity error	LE	DC accuracy	-	-	±0.1	%	
Differential linearity error	DLE		-	-	±0.1	%	
Digital input current high	I _{IHD}	-	-	-	5	μA	
Digital input current low	I _{ILD}	-	-0.1	-	-	μA	
Reference input current	I _{RIN}	V _{RIN} =-2.000V	-	-	10	μA	
Potential divider reference	Reference voltage	V _{ROUT1}	V _{EEA} = -5.20 V V _{VEED} = -5.20 V	-2.100	-2.000	-1.900	V
Band-gap reference	Reference voltage	V _{ROUT2}	-	-2.100	-2.000	-1.900	V
	Temperature coefficient	-	-	-	100	-	ppm/°C
Full-scale output voltage	V _{OFS}	-	-20	0	-	mV	
Zero-scale output voltage	V _{OZS}	V _{EEA} = -5.20 V V _{VEED} = -5.20 V V _{RIN} = -2.000 V	-2.068	-1.998	-1.928	V	
Output resistance	R _O	T _a =+25°C	192	240	288	Ω	
Power dissipation	I _{EE}	V _{EEA} = -5.46 V V _{VEED} = -5.46 V V _{RIN} = V _{ROUT1}	-59	-34*	-	mA	

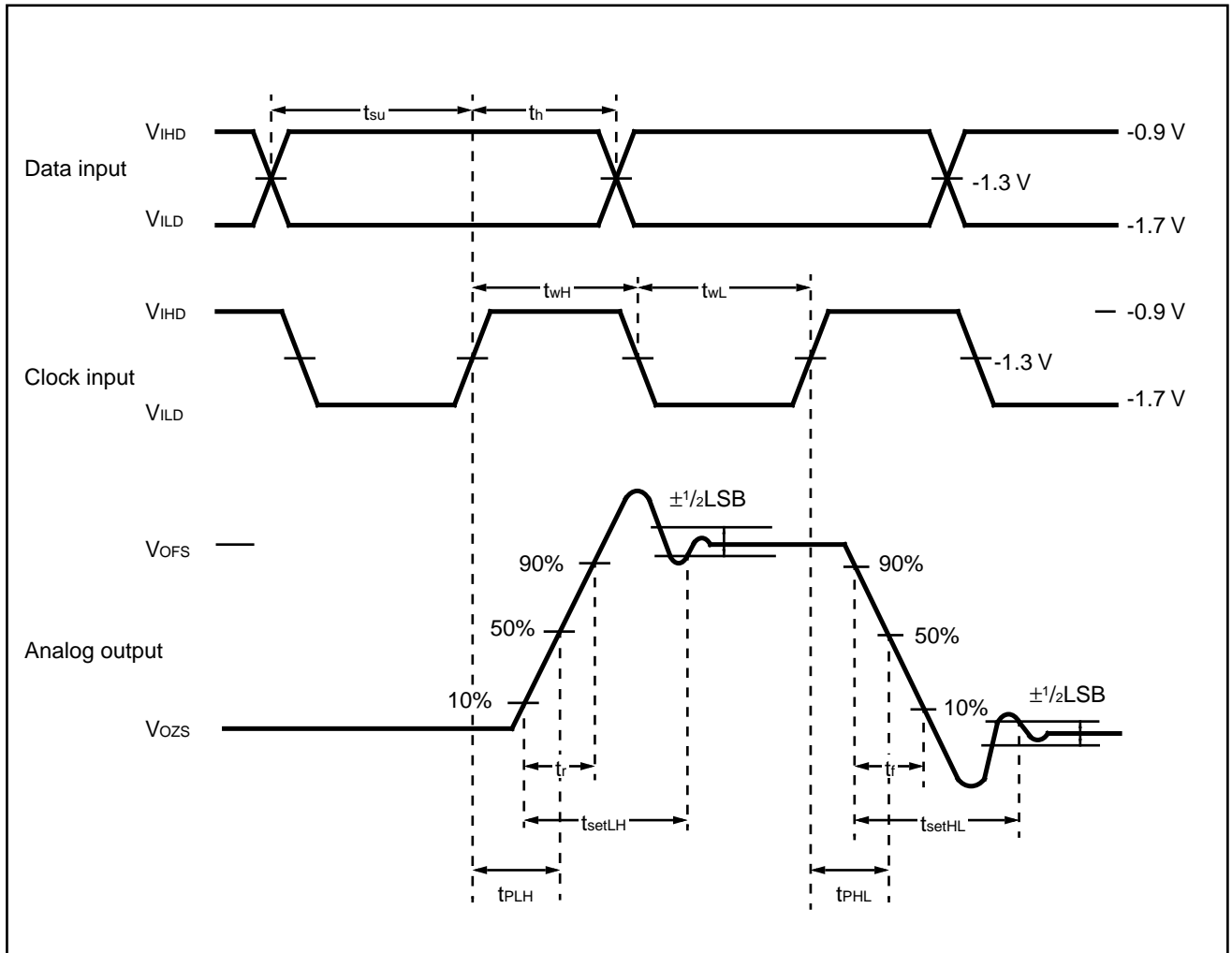
* : V_{EEA} = V_{VEED} = -5.20 V

■ AC CHARACTERISTICS

(V_{EEA}= V_{VEED}=-5.46 to -4.94 V, T_a=-20°C to +75°C)

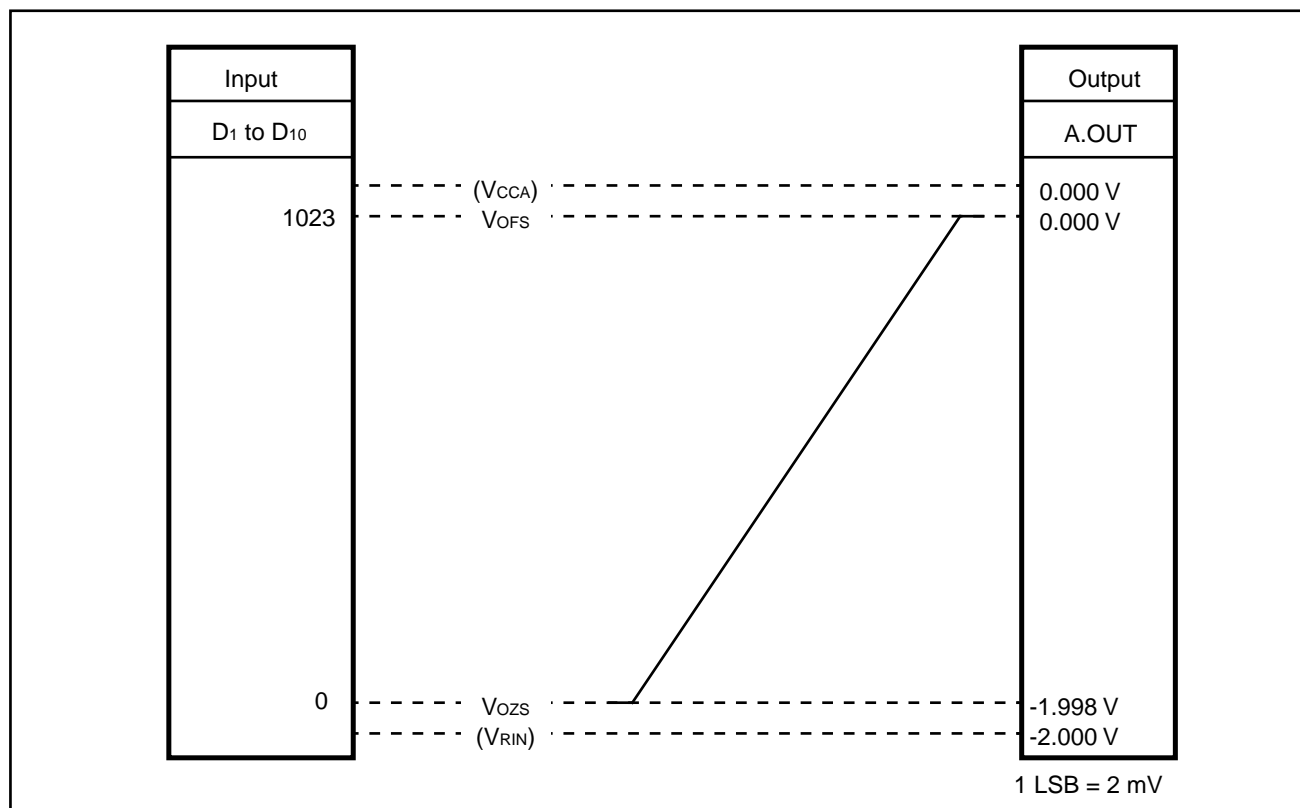
Parameter	Symbol	Conditions	Standard values			Unit
			Min.	Typ.	Max.	
Maximum conversion rate	F _S	CL = 15 pF A.OUT pin terminating resistance = 240 Ω	60	-	-	MSPS
Output propagation delay time	t _{pd}		-	7	-	ns
Output rise time	t _r		-	5	-	ns
Output fall time	t _f		-	5	-	ns
Settling time	t _{set}		-	17.5	-	ns

■ TIMING CHART



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■ DAC OUTPUT VOLTAGE CHARACTERISTICS



■ DAC OUTPUT VOLTAGE FORMULA IN IDEAL CONDITIONS

$$A.OUT = V_{CCA} - \frac{1023 - N}{1024} \times (V_{CCA} - V_{RIN})$$

(N : Digital input code from 0 to 1023)

$$V_{OFS} = V_{CCA}$$

$$V_{OZS} = V_{CCA} - \frac{1023}{1024} \times (V_{CCA} - V_{RIN})$$

NOTES

1. Preventing Switching Noise

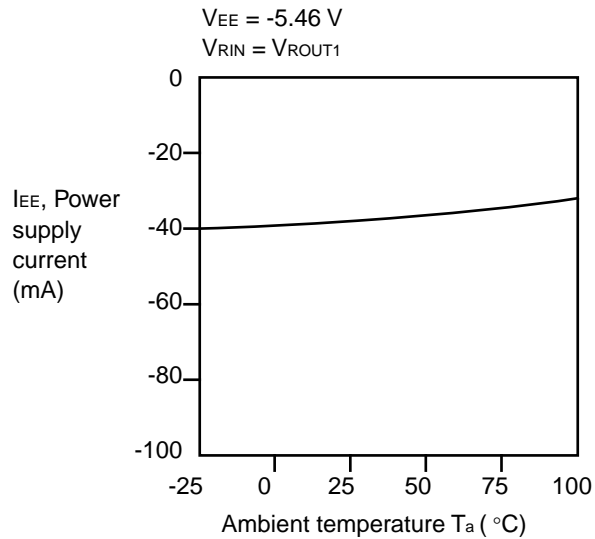
To prevent switching noise in the analog output signal, connect noise limiting capacitors to the V_{EEA} and V_{EED} pins as close to the V_{CCA} and V_{CCD} pins as possible.

2. Power Pattern

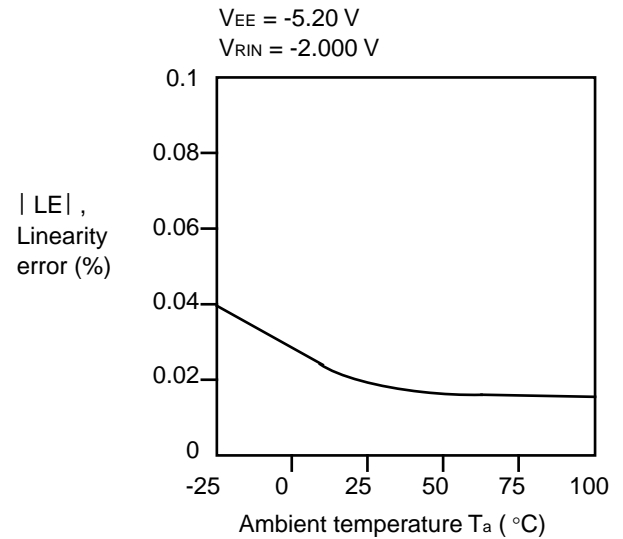
To reduce parasitic impedance, the PC board pattern to the V_{CCA} , V_{CCD} , V_{EEA} and V_{EED} pins should be as wide as possible.

■ TYPICAL CHARACTERISTICS CURVES

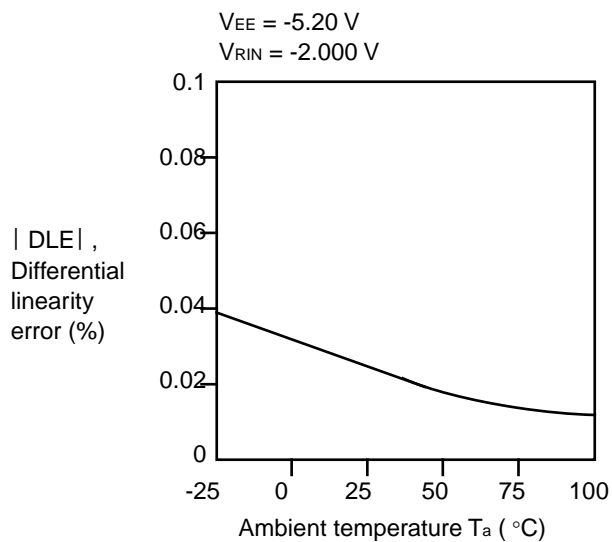
1. Power Supply Current v.s. Ambient Temperature



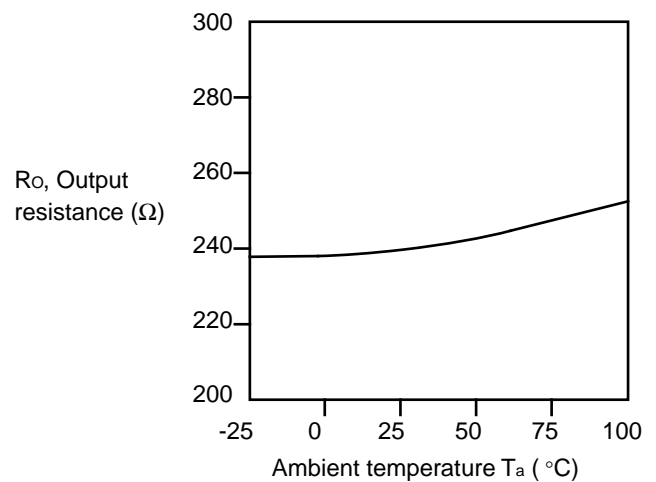
2. Linearity Error v.s. Ambient Temperature



3. Differential Linearity Error v.s. Ambient Temperature

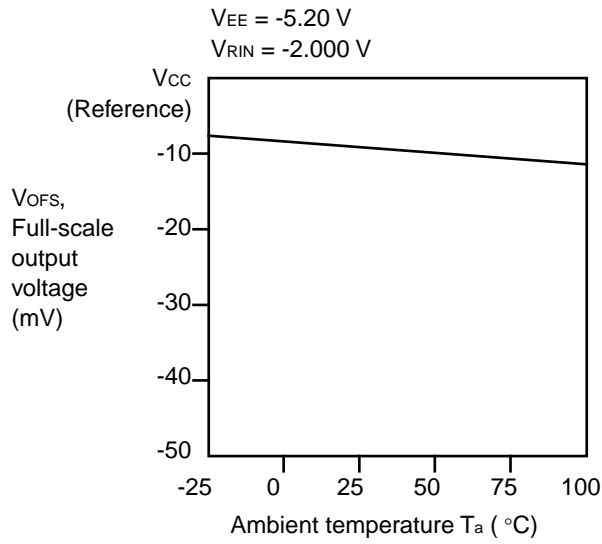


4. Output Resistance v.s. Ambient Temperature

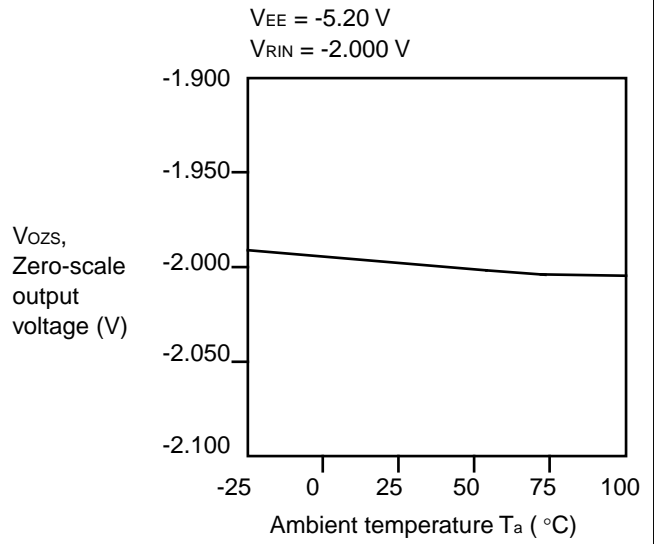


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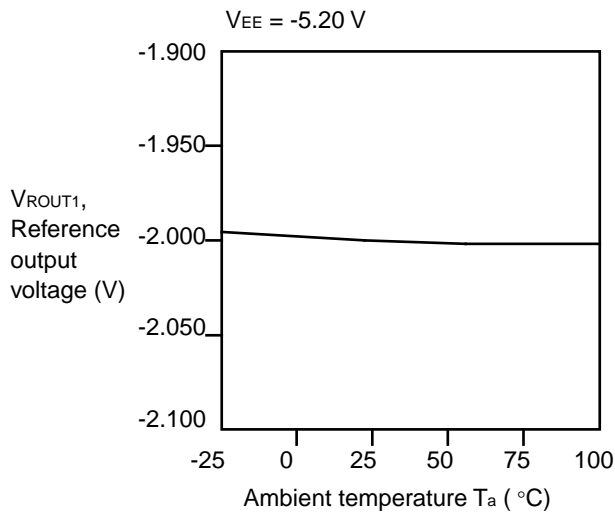
5. Full-Scale Output Voltage v.s. Ambient Temperature



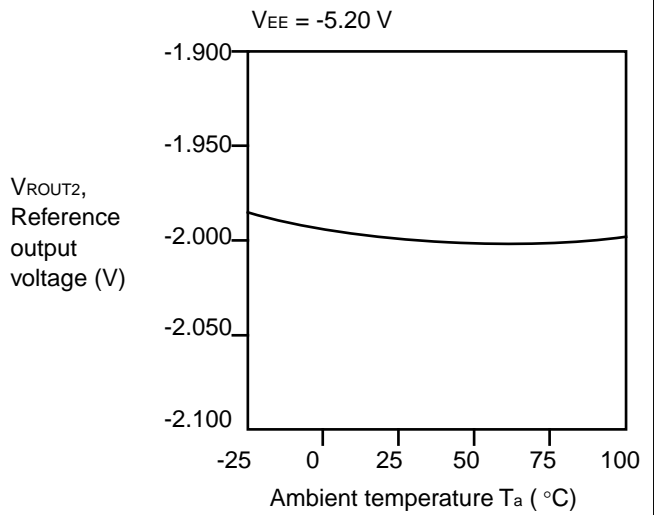
6. Zero-Scale Output Voltage v.s. Ambient Temperature



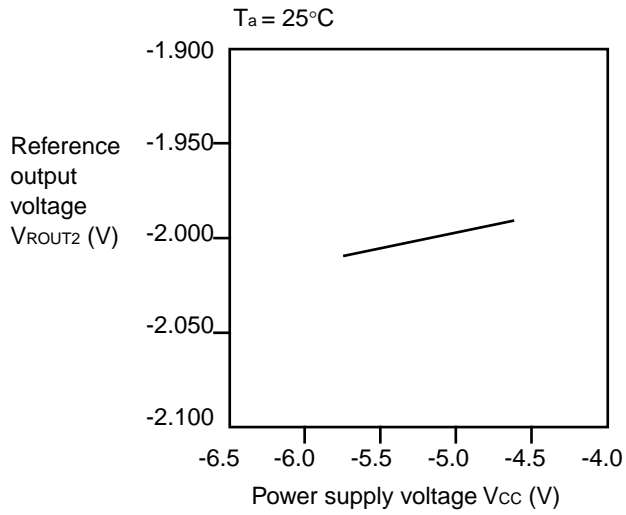
7. V_{ROUT1} Reference Output Voltage v.s. Ambient Temperature



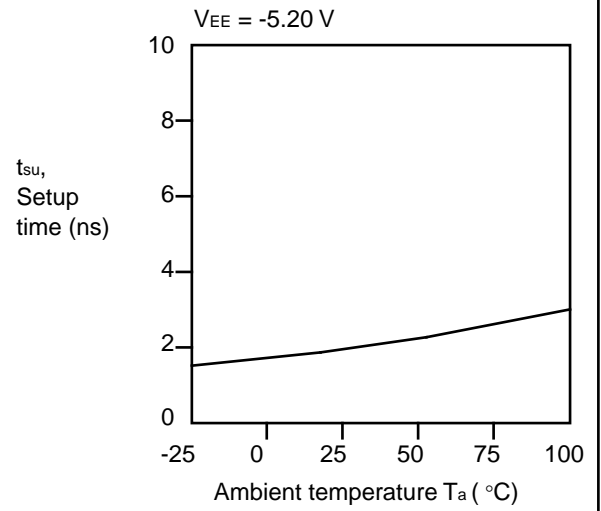
8. V_{ROUT2} Reference Output Voltage v.s. Ambient Temperature



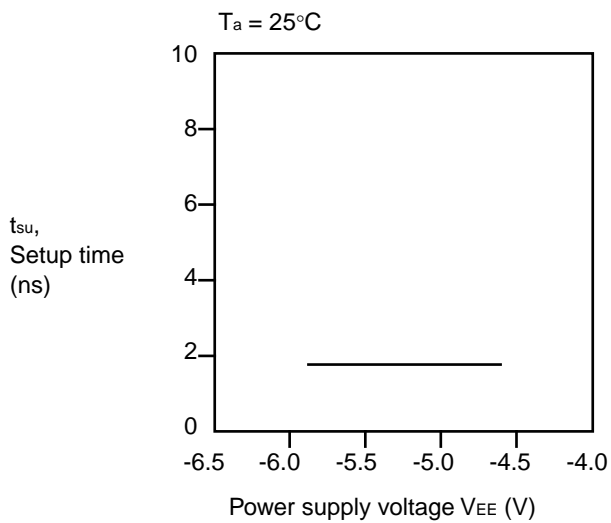
9. V_{ROUT2} Reference Output Voltage v.s. Power Supply Voltage



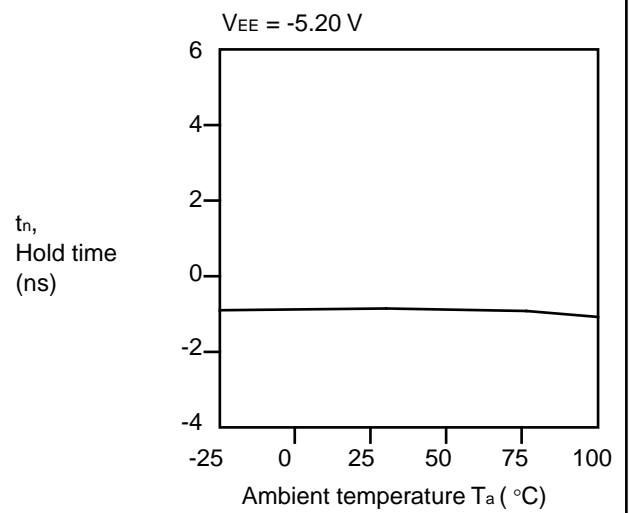
10. Setup Time v.s. Ambient Temperature



11. Setup Time v.s. Power Supply Voltage

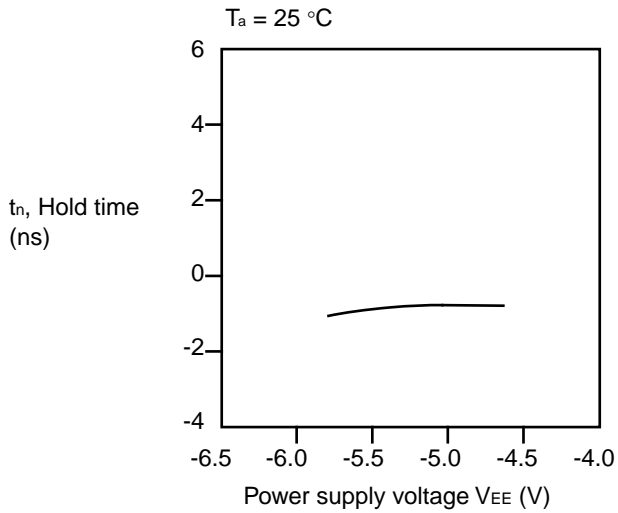


12. Hold Time v.s. Ambient Temperature

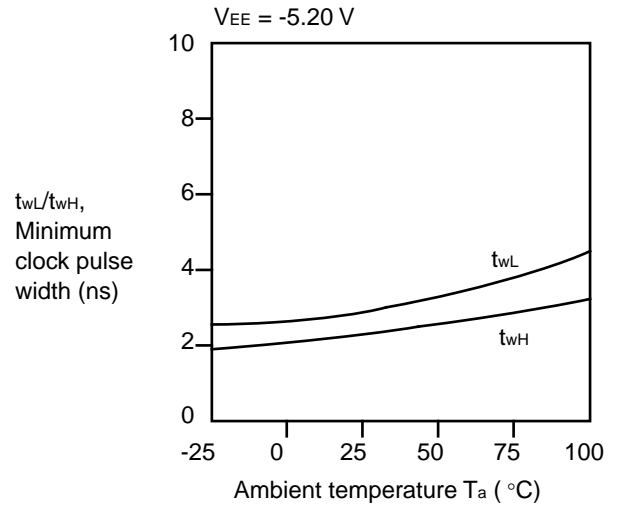


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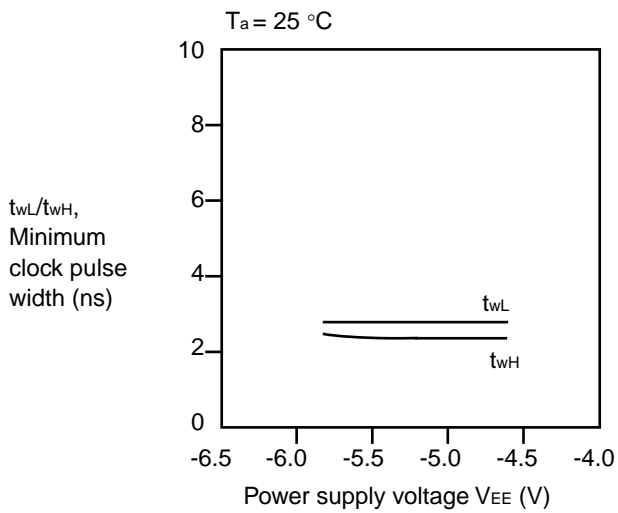
13. Hold Time v.s. Power Supply Voltage



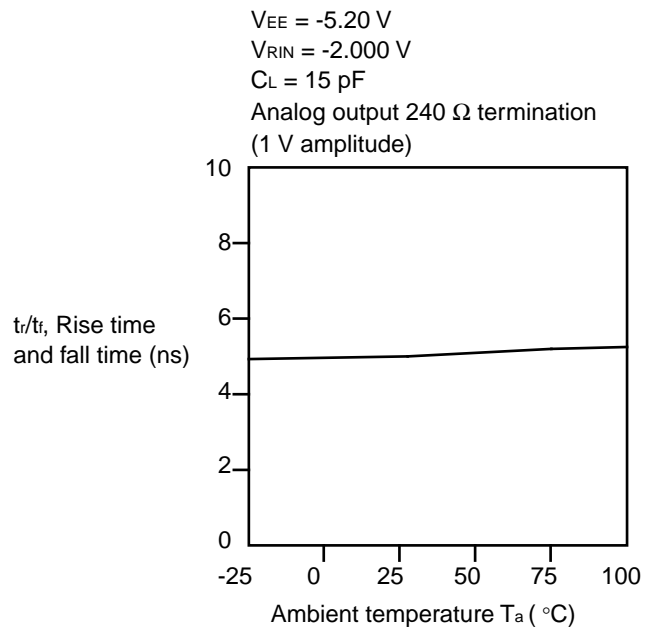
14. Minimum Clock Pulse Width v.s. Ambient Temperature



15. Minimum Clock Pulse Width v.s. Power Supply Voltage

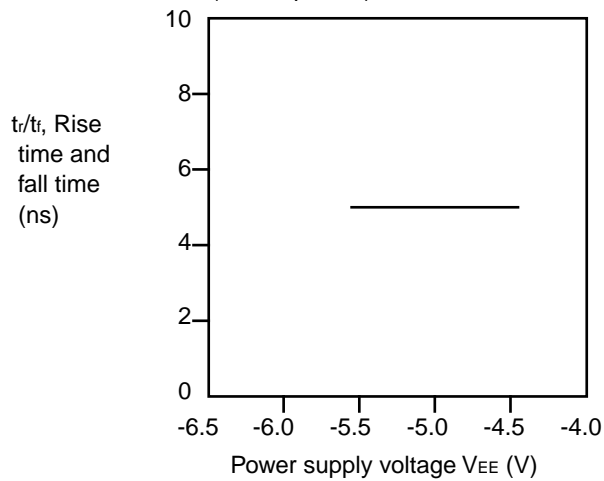
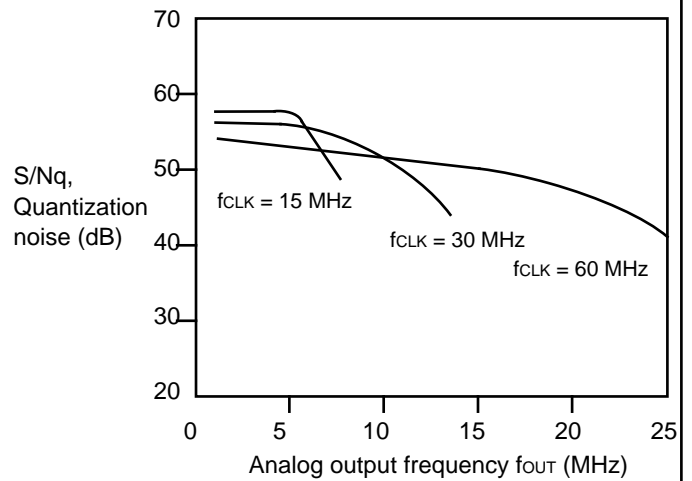


16. Rise Time / Fall Time v.s. Ambient Temperature



17. Rise Time / Fall Time v.s. Power Supply Voltage

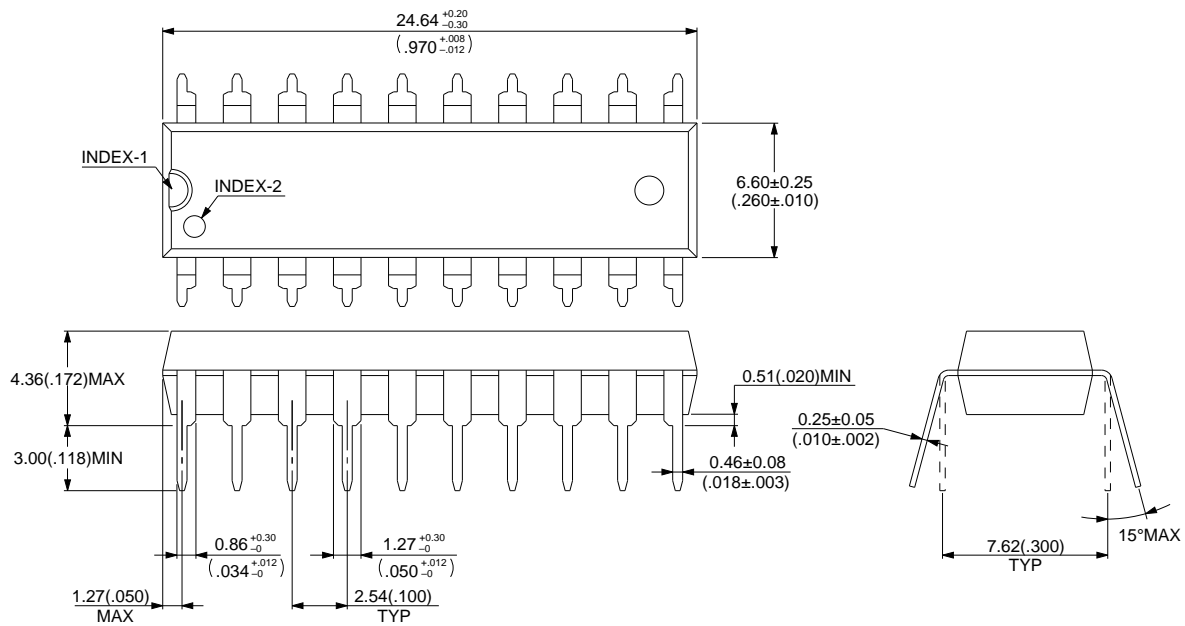
$T_a = 25\text{ }^\circ\text{C}$
 $V_{RIN} = -2.000\text{ V}$
 $C_L = 15\text{ pF}$
 Analog output 240 Ω termination
 (1 V amplitude)

**18. Quantization Noise v.s. Analog Output Frequency**

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■ PACKAGE DIMENSIONS

20 pins, Plastic DIP
(DIP-20P-M01)

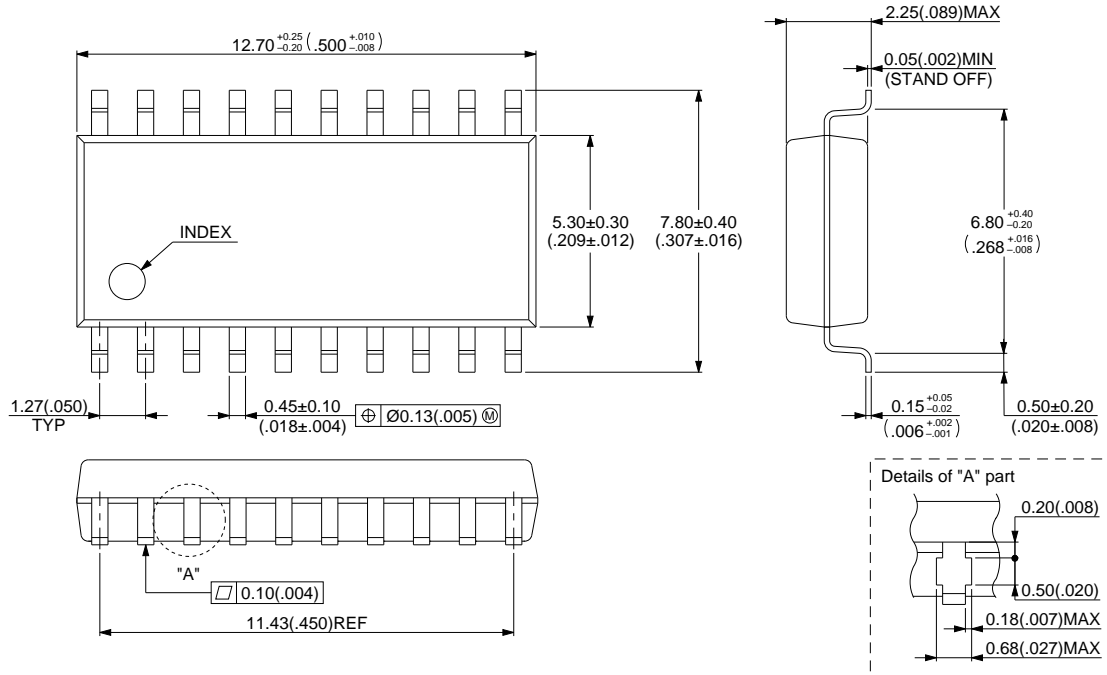


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Dimensions in mm(inches).

■ PACKAGE DIMENSIONS (Continued)

20 pins, Plastic SOP
(FPT-20P-M01)



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Dimensions in mm(inches).

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